forming a single layer dielectric lining on the surface of said first trench;

forming a spacer along the sidewall of said first trench over and in direct contact with said single layer dielectric lining;

forming a second trench into said substrate assembly at the bottom of said first trench by using said spacer as an etching guide;

forming a substantially uniform insulative material in said first and second trenches at least partially by substantially consuming said spacer and said single layer dielectric lining to substantially fill said first and second trenches with said substantially uniform insulative material.

30. (Amended) The process as recited in claim 25, wherein said step of forming said substantially uniform insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

31. (Amended) The process as recited in claim 25, wherein said insulative material and said dielectric lining are the same type material.

34. (Twice Amended) A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

forming a first trench into a semiconductor substrate;

forming a single layer dielectric lining on the surface of said first trench;

forming a semiconductive spacer along the sidewall of said first trench over and in direct contact with said single layer dielectric lining;

forming a second trench into said semiconductor substrate assembly at the bottom of said first trench by using said semiconductive spacer as an etching guide;

forming a substantially uniform insulative material in said first and second trenches at least partially by substantially consuming said semiconductive spacer and said single layer dielectric lining during formation to substantially fill said first and second trenches with said substantially uniform insulative material;

planarizing said substantially uniform insulative material;

wherein said process uses only one mask to form said device isolation.

37. (Amended) The process as recited in claim 34, wherein said step of forming said substantially uniform insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

38. (Amended) The process as recited in claim 34, wherein said substantially uniform insulative material and said single layer dielectric lining are the same type material.

40. (Twice Amended) A process for fabricating a semiconductor assembly having device isolation, said process comprising the steps of:

forming a mask over a silicon substrate assembly;

forming a first trench into said silicon substrate assembly using said mask as an etching guide;

forming an oxide layer on the surface of said first trench;

forming a silicon spacer on the sidewall of said first trench over and in direct contact with said single layer dielectric lining;

forming a second trench into said silicon substrate assembly at the bottom of said first trench by using said silicon spacer as an etching guide;

forming an oxide filler substantially devoid of other constituents in said first and second trenches at least partially by substantially consuming said silicon spacer and said oxide layer to substantially fill said first and second trenches with said oxide filler;

planarizing said oxide filler.

50. (Twice Amended) A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

forming a trench into a semiconductor substrate;

forming a single layer dielectric lining on the surface of said trench;

forming a semiconductive spacer along the sidewall of said trench over and in direct contact with said single layer dielectric lining;

forming substantially uniform insulative material in said trench at least partially by substantially consuming said semiconductive spacer and said single layer dielectric lining to substantially fill said trench with said substantially uniform insulative material.

53. (Amended) The process as recited in claim 50, wherein said step of forming a substantially uniform insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

54. (Amended) The process as recited in claim 50, wherein said substantially uniform insulative material and said dielectric lining are the same type material.

REMARKS

Favorable consideration of the application is respectfully requested. Claims 25-31, 33-38, 40-41, 43, 50-54 and 56, prior to this paper were pending in the present application. By this paper, claims 25, 30, 31, 34, 37, 38, 40, 50, 53 and 54, are amended.

Claim Rejections - 35 U.S.C. §112

Claim 25, prior to amendment, was rejected for insufficient antecedent basis.

The word "semiconductive" has been deleted before "spacer" in claim 25.

Therefore, by amendment, the rejection of claim 25 under 35 U.S.C. §112, second paragraph, is overcome.